

AMENDMENTS TO THE CLAIMS

The following is a complete list of all Claims in this Application (including withdrawn Claims). Cancelled and not entered Claims are indicated with Claim number and status only. The Claims listed below show added text with underlining and deleted text with strikethrough. The status of each Claim is indicated with one of (Original), (Currently amended), (Cancelled), (Withdrawn), (New), (Previously presented), or (Not entered).

Please AMEND Claims 21-22, in accordance with the following:

IN THE CLAIMS

1. (Original) A thin film transistor array panel comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode;

a first protrusion formed on the first passivation layer and disposed opposite the data line;

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and

a pixel electrode formed on the first passivation layer and connected to the drain electrode.

2. (Original) The thin film transistor array panel of claim 1, wherein the pixel electrode has a cutout.

3. (Original) The thin film transistor array panel of claim 2, further comprising a second protrusion disposed in the cutout.

4. (Original) The thin film transistor array panel of claim 2, further comprising a storage electrode line overlapping the pixel electrode.

5. (Original) The thin film transistor array panel of claim 4, wherein the storage electrode line comprises an expansion overlapping the drain electrode.

6. (Original) The thin film transistor array panel of claim 4, wherein the storage electrode line comprises a branch overlapping the cutout.

7-13. (WITHDRAWN)

14. (Original) A thin film transistor array panel, comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode and having a contact hole exposing the drain electrode at least in part;

a pixel electrode formed on the first passivation layer and connected to the drain electrode through the contact hole; and

a protrusion formed on the first passivation layer and disposed in the cutout at least in part.

15. (Original) The thin film transistor array panel of claim 14, further comprising a storage electrode line overlapping the pixel electrode.

16. (Original) The thin film transistor array panel of claim 15, wherein the storage electrode line comprises an expansion overlapping the drain electrode.

17. (Original) The thin film transistor array panel of claim 15, wherein the storage electrode line comprises a branch overlapping the cutout.

18. (WITHDRAWN)

19. (Original) The thin film transistor array panel of claim 14, further comprising a spacer having a height larger than the protrusion and disposed on the same layer as the protrusion.

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20. (Original) The thin film transistor array panel of claim 19, wherein the protrusion and the spacer comprise organic material.

21. (Amended) The thin film transistor array panel of claim 14, comprising a color filter disposed between the first passivation layer, and the protrusion and the pixel electrode.

22. (Amended) The thin film transistor array panel of claim 21, further comprising a second passivation layer formed on the color filter and intermediate to the protrusion and the pixel electrode.

23. (Original) The thin film transistor array panel of claim 1, wherein the semiconductor layer has substantially the same planar shape as the data line and the drain electrode.

24-27. (WITHDRAWN)

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